Design and Analysis of Broad-Band Fixed-Tuned Submillimeter-Waveguide Multipliers using MMIC Style Circuit Topology

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ABSTRACT

The design and analysis of varactor diode doubler, quadruple and cascaded doubler circuits for 320 and 640 GHz have been completed. A new approach has been employed to produce a tunerless waveguide mount with a very flexible, frequency scaleable, MMIC style multiplier circuit. The concept, design, predicted performance and measurements on some of the constituent mount elements are presented. Actual multiplier performance data is not yet available,

INTRODUCTION

In preparation for the instrument announcement of opportunity for the Far Infrared and Submillimeter Space Telescope, an ESA/NASA space astrophysics observatory mission, local oscillator sources at high frequencies (1200 GHz) arc being developed, As part of a multiplier chain beginning at -100 GHz, wc are developing single and multiple diode waveguide circuits up to 640 GHz. These multipliers arc expected to have high efficiency and broad bandwidth (20% fixed-tuned). This paper will describe the analysis, design and performance of broad band fixed tuned waveguide multipliers to 640 GHz

with enough output power to pump a quasi optical doubler providing 50 μW at 1200 GHz [1].

To take full advantage of available integrated device technology [2] and to meet the fixed-tuned bandwidth requirement, a new design approach for waveguide multipliers has been used. This approach employs input and output ridge-waveguide to micro strip transitions [3,4] to provide the fixed tuned input and output ports, and a single 'drop-in' MMIC style chip [5] containing the active devices and all matching elements. Several diodes can be used to increase the power handling, and/or to provide several multiplier stages on the same chip.

The new multiplier design has several advantages (in line input/output ports, fully integrated chip with room for matching and bias, simple and reproducible implementation, etc...), which will be discussed, The design has been verified through intensive use of computer numerical analysis tools such as MDS, MOMENTUM and HFSS [6]. An improved Schottky barrier diode model, including saturation effect [7], has been implemented in MIX, which takes into account the parasitic capacitance effects due to the diode contact finger structure. Analysis results for complete quadrupler and doubler circuits for 640 GHz will be shown and discussed. Although no performance data is yet available, RF measurements on some constituent elements of the multiplier mount will be given.

MULTIPLIER CONCEPT

The basic concept, used for ail our multiplier circuit variations - single and multiple diode doublers to 320 and 640 GHz, single and multiple diode quadruplers to 640 GHz and a cascaded multiple diode doubler chain to 640 GHz - is shown in Fig. 1. 'l'bin, metallic, ridge transitions, similar to those employed by [4], are used to couple the

input and output signals from fundamental waveguide to a microstrip mode. All other RF functions - frequency multiplication, matching and filtering - are then performed *on chip*. No tuning capability, other than adjustment of the bias voltage, is planned. The chip is held in place under the ridge transitions with a spring loaded mechanical micrometer drive assembly and no soldering is required. Wire bonds are used to couple bias into the chip through channels perpendicular to the input and output waveguide (not shown in the figure).

Because of their proven performance in this frequency range, we have implemented the multiplier circuits with planar Schottky barrier diodes, Our designs are based on the derived equivalent circuit of the T-anode diode (Fig. 2) which was first developed for oscillator [8] and later for mixer [2,9] applications. The T-anode devices have very low parasitic capacitance and lower than average series resistance compared to traditional planar varactors, making them ideal candidates for higher frequency circuits.

The diodes are matched to the waveguide input/output ports at the fundamental and harmonic frequencies through traditional microstrip elements - stubs and high/low impedance filters. Bias is coupled in through bypass capacitors formed on-chip. The complete circuit was designed to be implemented in GaAs but has the potential to be transported to a lower-loss lower-dielectric-constant substrate using the same transfer technique we have employed for our high frequency mixer circuitry [9]. To prevent undesired mode propagation in the GaAs chip we have kept the thickness small (<50 microns) and designed the ridge transitions to minimize waveguide mode coupling. Although unwanted mode propagation is a potential problem, we have seen no cause for concern in our simulations of the complete structure to date.

Since the approach we are taking involves significant risk, we have planned on implementing several multiplier configurations with similar circuit realizations to reach the 640 GHz output band. In the most traditional approach we are designing two separate

doubler mounts, the first operating over the 145-175 GHz band with an assumed input power of 15 mW, the second, doubling from 290-350 GHz with an assumed input power of 5 mW. This allows us to optimize individually, the frequency dependent wafer level characteristics for each multiplier stage, i.e. the doping profile. and chip size. The implementation which we feel has the most potential for producing high output power over wide bandwidths at high frequencies is the monolithic multiple-diode quadruple. This circuit is designed to operate with the same available input power as the cascaded doublers, 15mW at 145-170 GHz, but of course is implemented on a single wafer with much more complicated matching and filtering circuitry. Wafer doping profile and size arc traded off against circuit implementation but the computed available efficiency is still reasonably high. As a third implementation, wc have designed a circuit which cascades two doublers on the same chip. This has the disadvantage of compromising the doping profile but allows an integrated matching network to be inserted between the two doubler stages. The three circuit implementations are all realizable with the same device processing technology and are incorporated on the same or very similar mask sets. The waveguide block designs are also similar for the three multiplier cases. For brevity, we will focus only on the single-diode quadrupler circuit, although the approach is similar for al l of the multiplier configurations we have proposed.

ELECTRICAL DESIGN

Our approach consists in developing and optimizing circuit models for each functional clement of our multipliers using MDS, Momentum and HFSS and then to combine all the elements and simulate the complete structure, circuit plus waveguide mount. This approach is intended to speed up the design process by replacing the traditional scale model techniques and to offer more flexibility in analyzing variations during optimization.

Diode model

Beginning with the devices, we implemented a Schottky barrier diode model, including saturation effect [7], appropriate for the T-anode geometry, in MIX. This model is based on the diode geometry and equivalent circuit shown in Fig. 3. The electrical parameters of the diode arc described as a function of the epilayer doping N_d, the epilayer thickness t_{max}, and the anode dimensions, L and W. Both the voltage dependent conductance and capacitance arc implemented in MDS and corrected for current saturation. Using the diode mode], we were able to optimize the physical parameters of the diode, doping profile and anode geometry, for specific input power and frequency, and determine the optimum embedding impedances for each desired multiplier circuit configuration. The results for the single diode quadrupler arc given in Fig. 4.

Matching circuits

The matching circuit is the most difficult part of the design, but this is where the monolithic approach yields the most advantage, It must provide both filtering and impedance matching from the real impedance of the ridge transitions to the complex impedance of the diode, at the input, output, idler and higher harmonic frequencies. Fig. 5 shows such a circuit for a 1 diode quadruple to 640 GHz. First, because the diode is in series in the circuit, it must be shorted at both the input and idler frequencies on the output side (right of the diodes). Quarter wavelength open radial stubs provide these shorts. Similarly, another stub shorts the diode at the output frequency on the input side (left of the diodes). A hammerhead low pass filter at the input provides a reactive impedance at each harmonic (320, 4S0 and 640 GHz) and prevents generated power from leaking back out the input port. Bias enters through a bypass capacitor before the low pass filter and a simple" step transformer matches the 30 Ohm microstrip to the input waveguide ridge transition. Bet wccn the hammerhead filter and the diode, a high/low

impedance transformer matches the 30 Ohm impedance of the filter to the optimized diode impedances at 160 and 320 GHz. On the output side, three more open stubs match the diode impedance at 640 GHz to the final 50 Ohm microstrip line which couples to the output waveguide ridge.

In our first design iteration, we used microstrip lines and distributed elements for the filters and impedance matching. As we will show later, this approach dots not allow us to realize a predicted bandwidth above 15% (our goal is 20%). We are currently working on a second iteration utilizing some lumped elements and coplanar waveguide which we hope will result in increased bandwidth.

Ridge Transition

The most common method of forming waveguide to microstrip transitions at high frequencies is to use traditional centered waveguide probe transitions. These transitions require very narrow probe dimensions and very thin support substrates at 600 GHz and can limit circuit flexibility when designed to prevent undesirable waveguide mode propagation. An alternative concept, which we believe is better suited for MMIC style chips, was proposed for the microwave bands in [3] and used very successfully at 80 GHz by [4]. It consists of a Tchebysheff impedance transformer formed from a metallic stepped ridge transition. By forming the transition separately from the waveguide block, we have been able to implement this design quite easily at 640 GHz. The ridge mates to the GaAs circuit chip via a pressure contact to the conductor layer of the 30 ohm microstrip line.

The ridge transition design is based on impedances given in [10] that we have corrected using HFSS. The impe.dance difference bet ween the waveguide mode (-500 Ohm) and the microstrip mode (50 Ohm) is matched using a Tchebysheff step transformer, for which the quarter wavelength long steps are modified slightly to correct

for the end reactance. The transformer uses three ridge steps, with the fourth step being the ridge to microstrip transition. The ridge thickness and microstrip line impedance arc optimized within certain constraints to give the best match at the input and output frequency.

The ridges arc fabricated from BeCu using a double sided photoetch technique. "I'he 160 GHz ridge is formed from .003" BeCu and the 640 GHz ridge from .0015" sheet, The sheets, containing many ridges, are etched in ferric chloride and then gold plated. We obtained an accuracy of 2-7 μm for the dimensions, After separation from the "spider mount" (Fig. 6) the individual ridges can be readily handled and arc. soldered into position permanently in the waveguide mount.

Measurements of the transmission properties of the ridge were performed in a test mount at 160 GHz. A simple split block with WR7 waveguide input and output, and a chip relief in between, was fabricated and a 30 Ohm straight microstrip line was formed on GaAs for insertion under the ridges (Fig. 7). The measured transmission through the two transitions and the wafer are shown in Fig. 8a, For comparison the wafer has been removed in Fig. 8b and the ridge-to-ridge interaction can be seen (resonance near 155 GHz in both curves). When the measured waveguide loss of .5 dB and calculated substrate loss of 1 dB arc subtracted, the ridge transitions show an insertion loss of only ,25 dB each. We have also simulated the complete structure in HFSS (red curves in Fig. 8) which yields excellent agreement in the case of the waferless circuit but poorer agreement when the microstrip circuit is present. We believe this is partially due to the difficulty of making good electrical contact to the ridges in the test block which did not have the capability to push the ridges firmly up against the chip.

Waveguide Mock

The 160-640 GHz quadrupler mount which contains the ridge transitions and multiplier chip is shown in Fig. 9. It is formed in three parts, two of which are used to permanently fix the ridges in place at the center of the wave.guide, A separate top piece protects the chip and, when removed, allows access for positioning and wire bonding the bias line during assembly. The output waveguide is followed by a channel waveguide transformer to square waveguide and an integrated Potter horn [11], The waveguides and transitions arc formed in the split block, but once the ridges have been positioned and soldered in place the two halves arc permanently mated. Insertion of the GaAs chip is made possible by a novel spring loaded moving, post controlled by a micrometer with a simple cam mechanism. During contacting, the chip is placed in position in a recess under the two ridges and raised into final position where it is pressed against the ridges. Once the contact is made, the micrometer is locked and no further adjustments are required.

COMPUTED PERFORMANCE

We have carefully analyzed the individual elements of each of the multiplier designs wc arc implementing using HP's MDS, Momentum and HFSS programs. Specific circuit elements were optimized and then combined into a full structure model. The S parameters for the ridge-waveguide to microstrip transition were computed using HFSS and then imported to MDS. The microstrip circuits were described using MDS models, but HFSS simulations have been performed to check the accuracy of those models. Good agreement is found, except at 640 GHz, where wc are outside the bounds of the MDS element models. At this frequency the open stubs show some radiation (-1.2 dB) which cannot be eliminated without reducing the substrate thickness. Both the ridge and the microst rip circuit S parameters arc inserted in an M DS model, which also contains the diode physical model with the optimized geometric parameters. In the

simulations, the diode doping level was fixed at 3×10^{17} cm^{-3} so that all the circuits could be made on similar and available GaAs wafers. It should be noted that this doping level is close to optimum only for the two-diode quadrupler design.

Fig. 10, shows the performance for the different multiplier configurations considered at the design center frequency and expected input power level. The performance predictions include the saturation effect and known diode parasitic, such as the pad-to-pad and finger-to-pad capacitance. The computations optimize the anode geometry and embedding impedances to maximize the efficiency, and therefore the output power.

It can be seen that the predicted single device quadrupler performance is fairly realistic. We obtain an efficiency of 3.8%, whereas measured data for quadruples around this frequency using whiskered diodes is reported to be around 2% [12]. Two single-device doublers in cascade show better overall performance, but of course with twice the number of devices. Finally, a two-diode quadruple shows the best efficiency. Potentially, the cascaded doublers are easier to design and can achieve higher overall efficiency, as the device parameters can be optimized individually for each frequency range, but they require more devices in total and might suffer from interactions between the two stages. Although the quadruples are more difficult to design, they don't have a stage-to-stage interaction problem and can potent iall y give the same overall performance efficiency as chained doublers.

Fig. 11a and 11 b show more detailed computed performance data for a single diode quadrupler. The output efficiency and power vs. input power and frequency are plotted under fixed tuning conditions, and fixed bias in the frequency sweep case. The achievable bandwidth is apparent in the frequency plot, where the goal of 20% is not quite met. This may be correctable with an improved circuit implementation, which wc arc currently working on. Also it can be seen in the efficiency versus input power curve,

that the saturation of the diode doesn't occur at 15 mW, as it has been optimized for, but at 20 mW. 'l'his is due to an imperfect match of the input circuit to the diode. This mismatch is due to the difficulty of matching simultaneously both the input signal and the idler with the same circuit. Having a mismatch at the input frequency leads to a smaller absorbed power, but a mismatch at the idler leads to a lower conversion efficiency. We have chosen the first option in this design. Again, improvements may be possible in subsequent iterations.

CONCLUSION

We have presented a new multiplier design which has several advantages: in-line input/output ports, a fully integrated chip with room for matching and bias, a readily scaleable design, simple handling and mount integration, etc . . . . The design has been verified through extensive use of numeric analysis tools such as MDS, MOMENTUM and HFSS. An improved Schottky barrier diode model, including saturation effect and known diode parasitic, has been implemented in MDS. High frequency waveguide ridge transitions arc used to provide tunerless wide band performance in a waveguide mount, and have been fabricated both at 160 and 640 GHz, with good dimensional accuracy. Measurements on back-to-back transitions at 160 GHz show excellent performance and reasonable agreement with simulations, A new block design, which simplifies device handling and assembly, has also been realized and fabricated, Circuit chips arc currently in fabrication and the first 640 GHz measurements are expected very soon. The design approach can be extended readil y to other submillimeter- wave devices, such as mixers, detectors or amplifiers. In the long term, complete integration of receivers can be imagined.

ACKNOWLEDGMENTS

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[12] Neal Erickson, private communication.

FIGURES
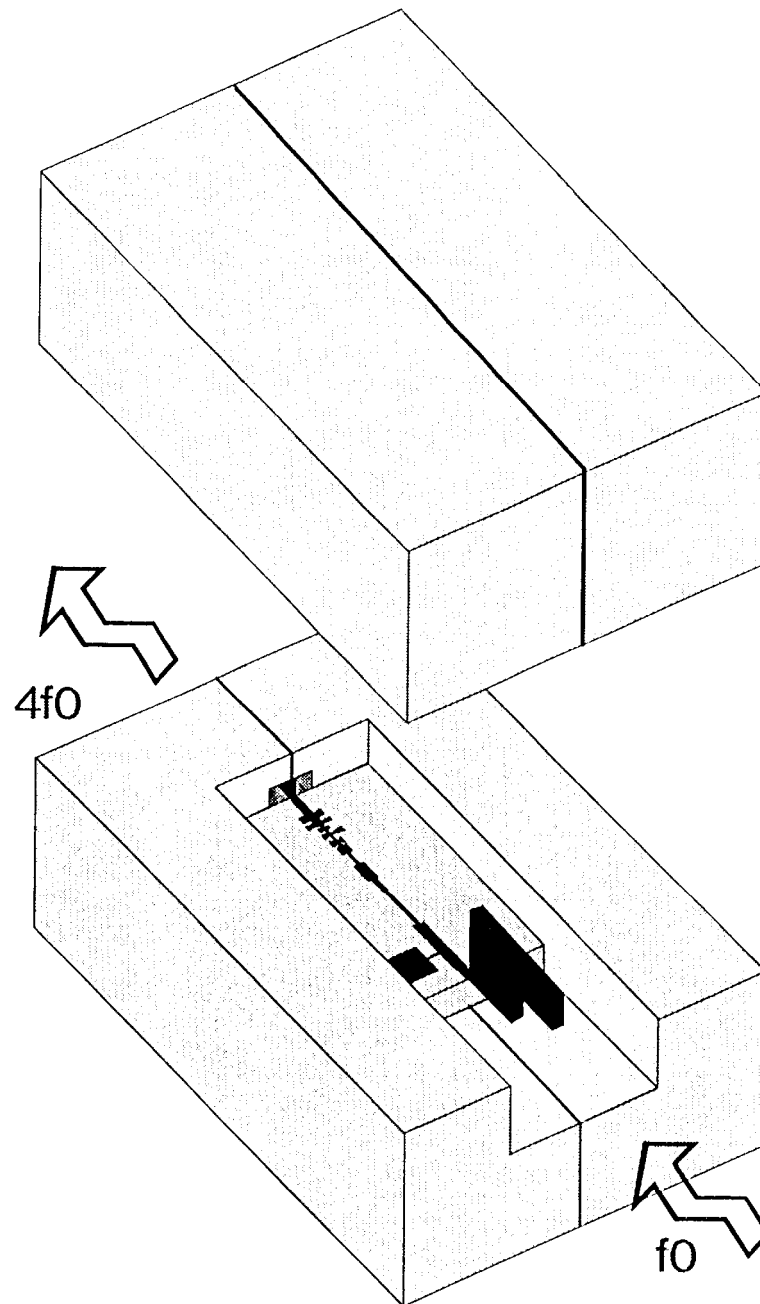
Fig 1. General concept of the broad band tunerless waveguide multiplier with MMIC style circuit.
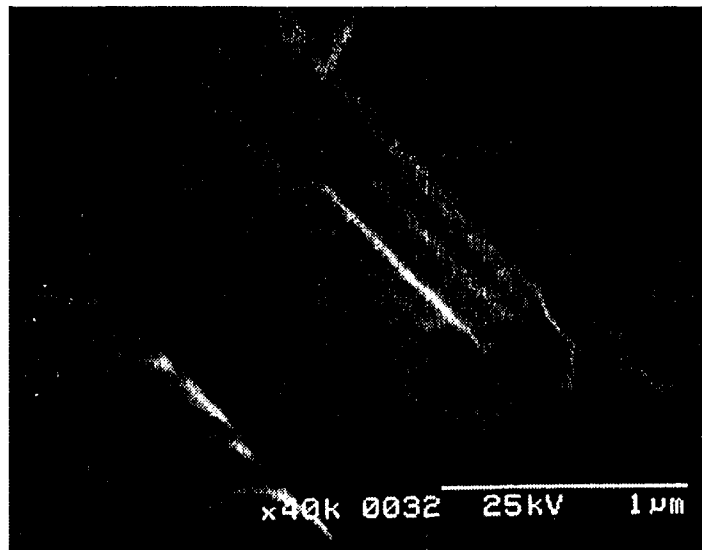
Fig 2. SEM photographic of a T-anode Schottky diode fabricated in the JPL Micro Devices Laboratory (MDL).
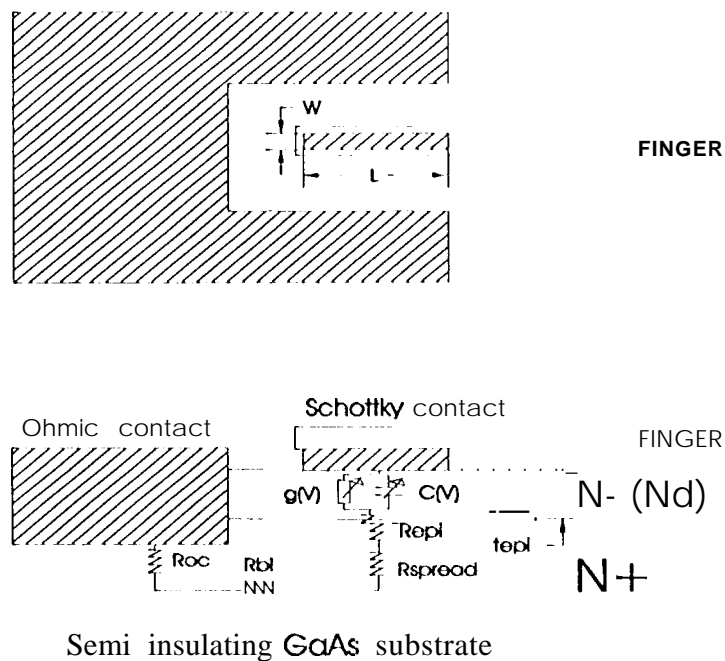

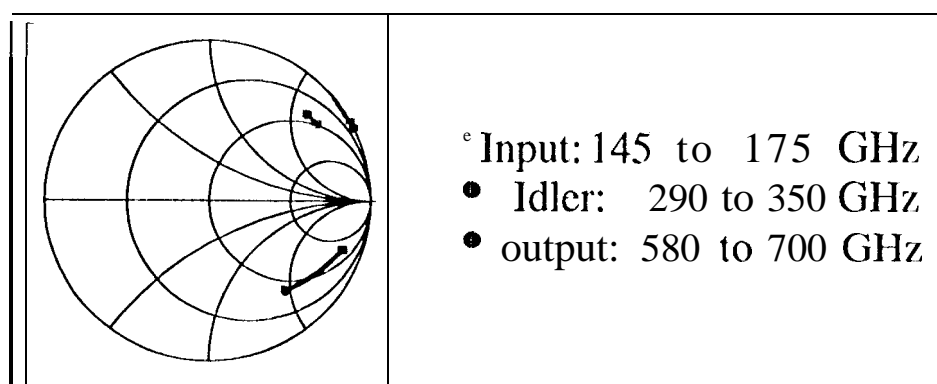Fig 3. Geometrical and electrical model used to optimise the T-anode Schottky diode in MIX.

° Input: 145 to 175 GHz
• Idler: 290 to 350 GHz
• output: 580 to 700 GHz

Fig 4. Diode Embedding impedances for a quadruple to 640 GHz: Fin= 160GHz, Pin=15mW, L=1 Oum, W= 1um, Nd=3e17cm-3.

Bias

Diode

Parallel matching circuit at 640 GH

Hammer- High-Low impedance matching
Head   at input and idler frequencies
Low-pass   (160 and 320 GHz)
Filter

Short at 640 GHz

Short at 160
and 320 GHi

Chip 1.65x3.53 mm
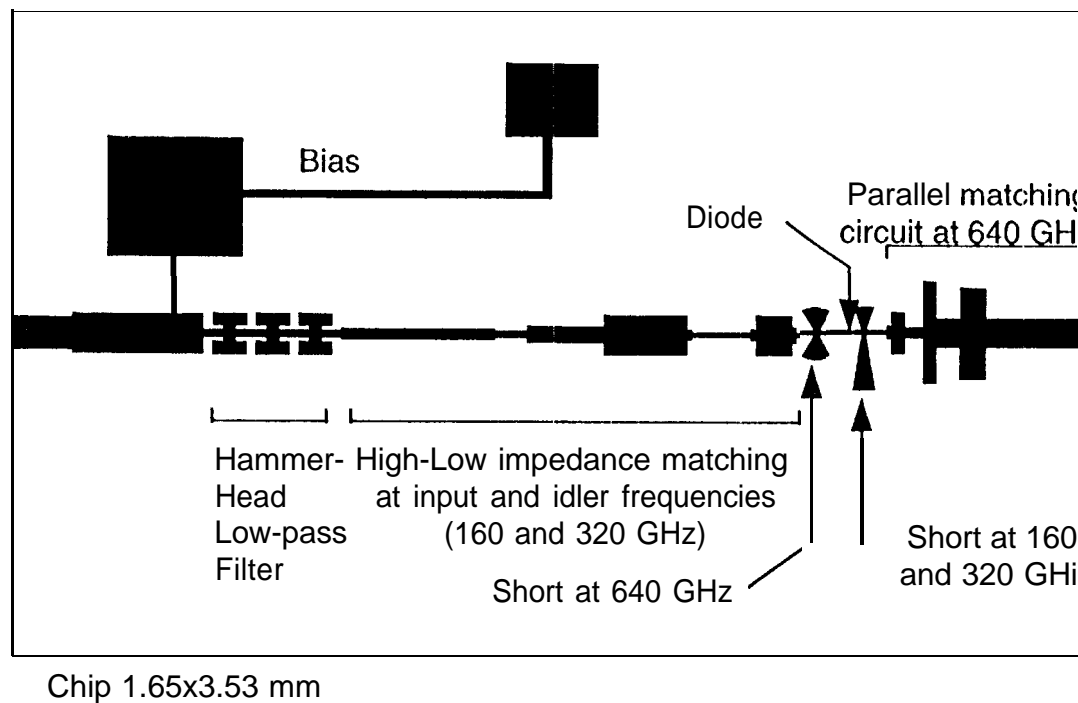
Fig 5. Circuit layout of the 1 diode quadrupler to 640 GHz.
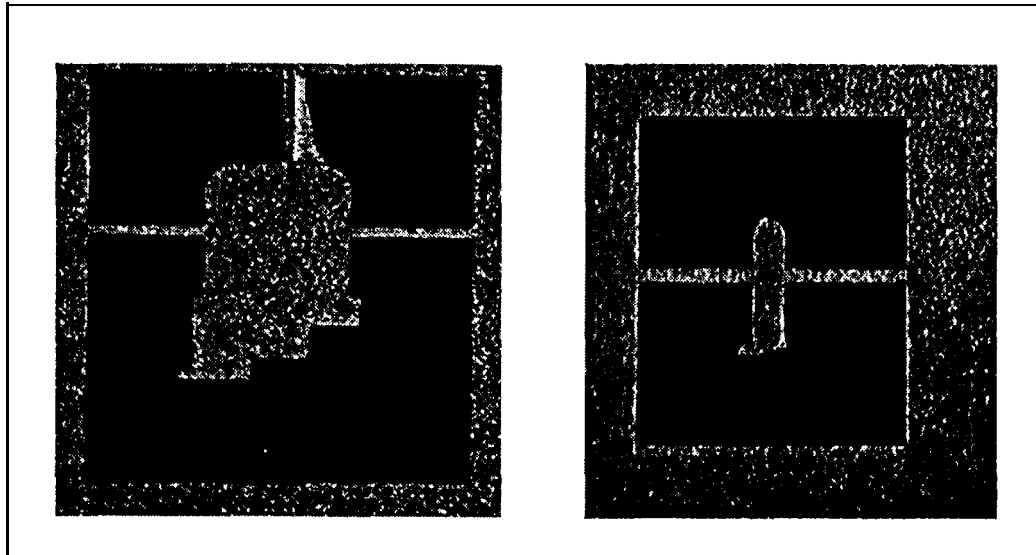
Fig 6. 160 GHz and 640 GHz waveguide ridges for transition from waveguide to microstrip: the 160 GHz ridge is on a 76 um thick BeCu sheet, the 640 GHz on a 38 um. They are both gold-plated.
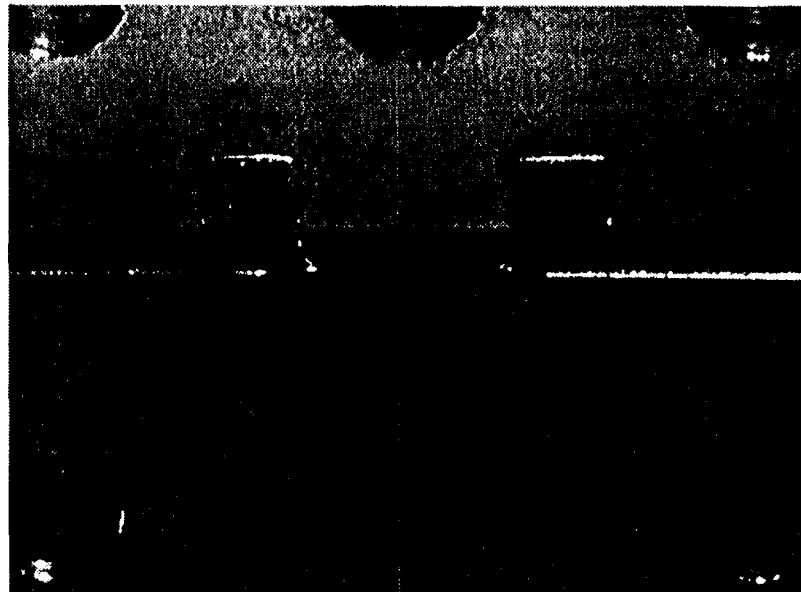
Fig 7. Test block for the measurements of the 160 GHz waveguide ridge to microstrip transition. In a WR7 Waveguide, two ridges contact a 30 Ohms line on GaAs.
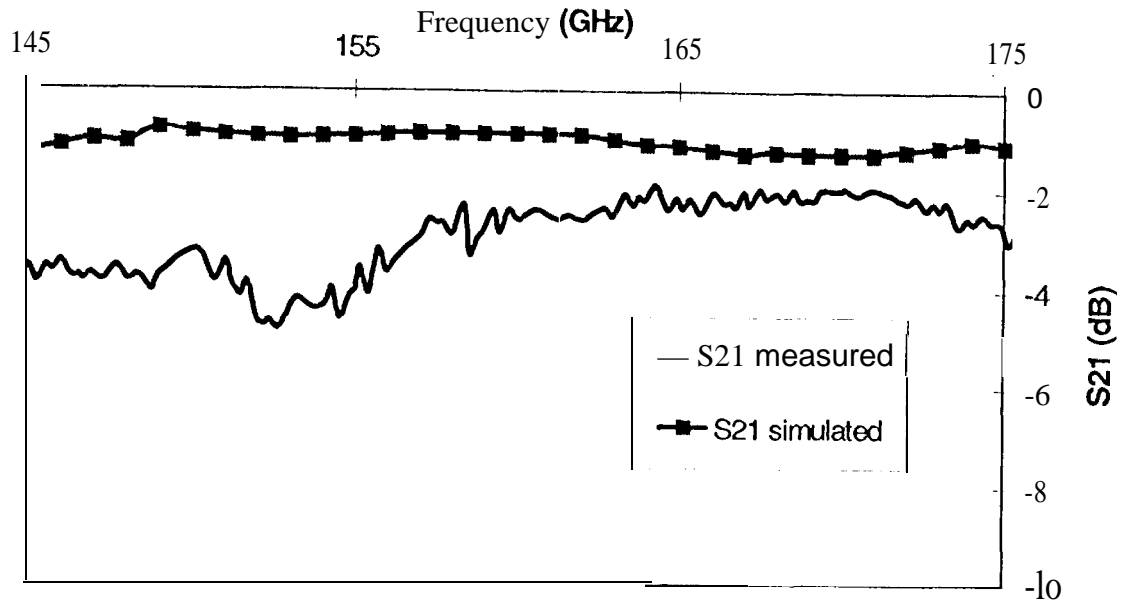
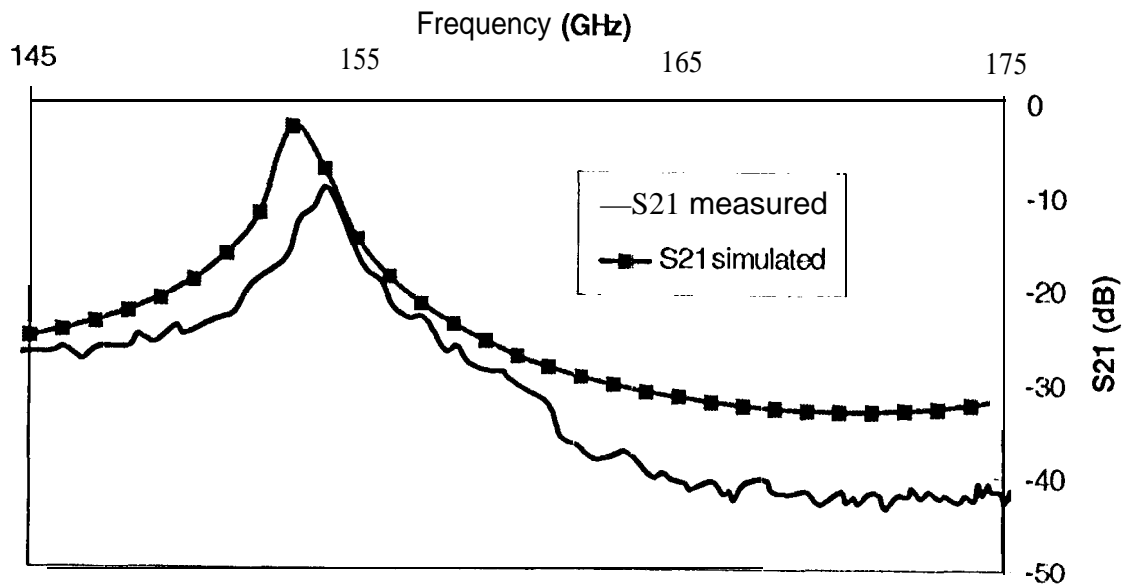Fig 8a, Measured and simulated transmission for wo ridge contacted to a 30 Ohms line in a WR7 waveguide.

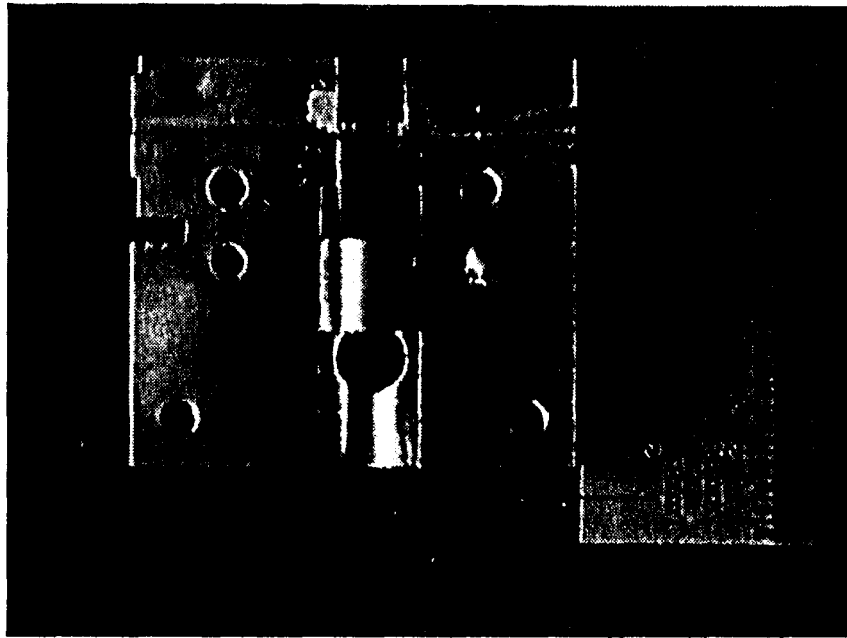Fig 8b. Measured and simulated transmission for two ridge *without* line in a WR7 waveguide.

ïg 9. Picture of the block for the 640 GHz quadruple: are shown a 160 GHz ridge in the input waveguide, a 640 GHz ridge in the output waveguide, and a chip on the mobil post.

Input: doping=3e1 7, Pin=15m W at 160 GHz

Includes: saturation effects, known parasitic effects (finger)

Program optimizes: Anode geometry to maximize output power

- Quadruple to 640 GHz, 1 device:
    efficiency=3.8%, Output Power=500 UW
- Two chained doublers to 640 GHz, both one device:
    (doubler to 320 GHz: eff=40%, Pout=6 mW, doubler to 640 GHz: eff=30%, Pout=1.8 mW)
    efficiency=1 3%, Output Power=1.8 mW
⟹ Quadrupler to 640 GHz, 2 devices in seri:
    efficiency= 18%, Output Power= 2.7 mw

Fig 10. Comparative performance of the different multipliers configuration, for given operating parameters.
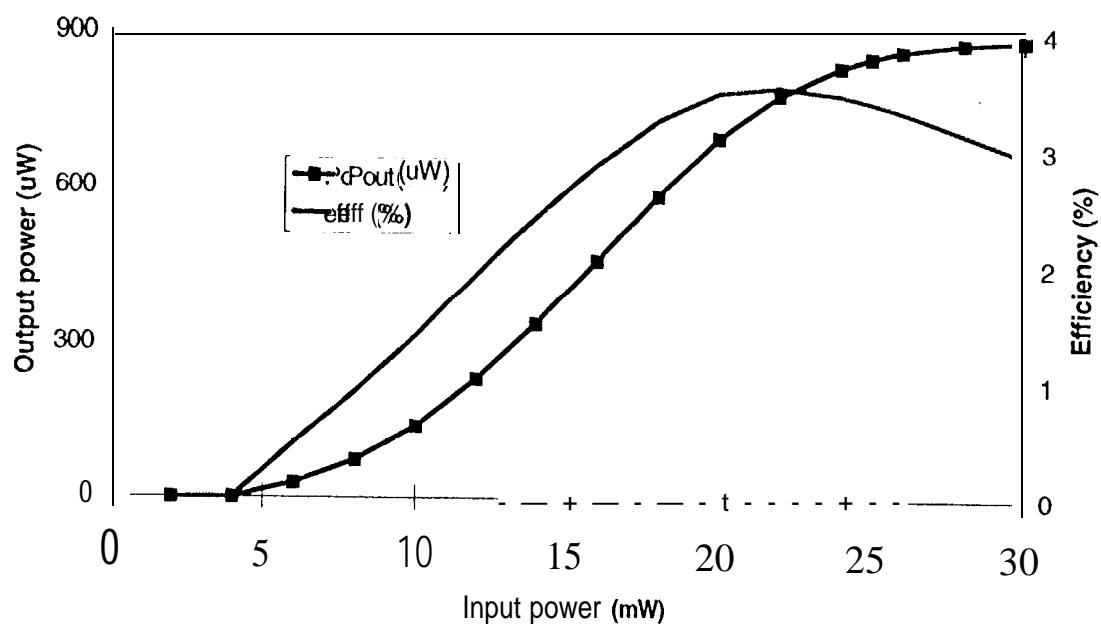
Fig 11a. Output power of the complete 1 diode quadrupler versus input power with an input frequency of 160 GHz.
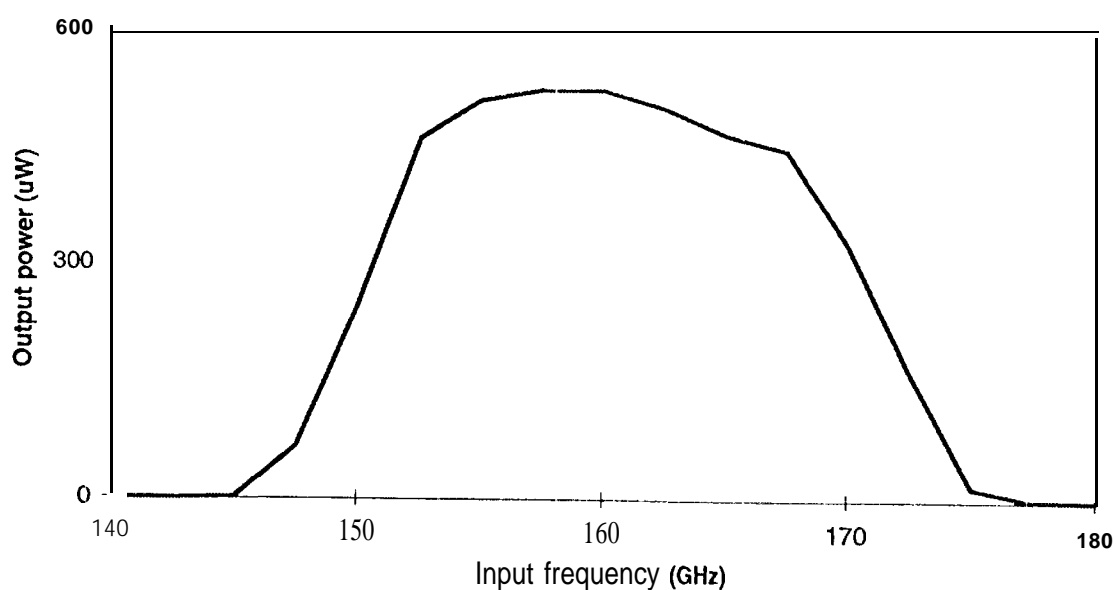

Fig 11 b. Output power of the complete 1 diode quadrupler versus input frequency with an input power of 15 mW.